

DEVICES HAVING IMPROVED CAPACITANCE AND METHODS OF THEIR FABRICATION

Background

Although there have been attempts to deposit metal oxides, such as TiO_2 and SrTiO_3 , during semiconductor fabrication, thermal oxidation of metals in the fabrication of capacitors has been limited since an initial oxide layer prohibits further diffusion during thermal oxidation. As a result the use of high dielectric constant oxidized metals has been limited in semiconductor capacitor fabrication. One such metal, titanium dioxide, has a dielectric constant 2-15 times greater than present semiconductor capacitor dielectrics such as silicon nitride, while titanates are 2-1000 times greater.

In the January 1996 issue of Material Research, Vol. 11, No. 1, an article entitled ELECTROCHEMICAL SYNTHESIS OF BARIUM TITANATE THIN FILMS, R.R. Bacsa et al. describes the synthesizing of polycrystalline films of barium titanate on titanium substrates by the galvanostatic anodization of titanium to form a material which has a dielectric constant of 200.

Summary of the Invention

The invention includes new capacitor structures and dielectrics and methods for forming such capacitors and dielectrics.

In one exemplary embodiment the capacitor of the invention is formed by a process using only two deposition steps. The capacitor has first and second conductive plates and a dielectric is formed from the first conductive plate.

In one exemplary process in accordance with the present invention a metal layer is deposited and at least partially oxidized in an electrolytic solution. The metal oxide formed during this oxidation forms the dielectric of the capacitor. Portions not oxidized may form at least a portion of a capacitor plate.

In one exemplary implementation in accordance with the present invention, a metal layer is deposited to overlie a first capacitor plate fabricated on a semiconductor wafer. The wafer is placed in an electrolyte conducive to forming an oxide with the metal. A potential is applied across the electrolyte and the metal, and at least a portion of the metal oxidizes. In a preferred embodiment the metal is titanium and titanium dioxide is formed during the electrochemical reaction. The capacitor fabrication is completed with the formation of a second capacitor plate overlying the oxidized metal layer. The oxidized metal layer functions as the dielectric of the capacitor and has a high dielectric constant.

Brief Description of the Figures

Figure 1 is a cross section of a semiconductor wafer following the formation of a silicon dioxide layer and the masking thereof.

Figure 2 is the cross section of Figure 1 following an etch of the silicon dioxide layer and following a deposition and etch of polysilicon.

Figure 3 is the cross section shown in Figure 2 following a deposition of titanium.

Figure 4 is the cross section shown in Figure 3 when placed in an apparatus configured to perform electrochemical oxidation.

Figure 5 is the cross section shown in Figure 4 following the oxidation of the titanium layer.

Figure 6 is the cross section shown in Figure 5 following the deposition and masking of a conductive layer.

Figure 7 is the cross section shown in Figure 6 following the final capacitor formation.

Figure 8A is the cross section of the semiconductor wafer shown in Figure 1 following an etch of the silicon dioxide layer and a deposit of a first metal layer.

Figure 8B is the cross section of the semiconductor wafer shown in Figure 1 following an etch of the silicon dioxide layer and a deposit and planarization of a first metal layer.

Figure 9A is the cross section shown in Figure 8A following the electrochemical oxidation of the first metal layer and a deposit of a second metal layer.

Figure 9B is the cross section shown in Figure 8B following the planarization and electrochemical oxidation of the first metal layer and following a deposit and planarization of a second metal layer.

Figure 10A is the cross section shown in Figure 9A following an electrochemical oxidation of the second metal layer.

Figure 10B is the cross section shown in Figure 9B following a electrochemical oxidation of the second metal layer.

Figure 11A is the cross section shown in Figure 10A following the formation of a capacitor plate and the masking thereof.

Figure 11B is the cross section shown in Figure 10B following the formation of a capacitor plate and the masking thereof.

Figure 12A is the cross section shown in Figure 11A following an etch and showing one capacitor of the invention.

Figure 12B is the cross section shown in Figure 11B following an etch and showing one capacitor of the invention.

Figure 13 is a block schematic of a memory system of the invention.

Detailed Description of the Preferred Embodiments

Figures 1-7 depict cross sectionally a semiconductor wafer 1 following the process steps of a first embodiment used in fabricating the wafer 1. In Figure 1 field oxide regions 2 and wordlines 3 have been formed overlying a substrate 4 using conventional semiconductor process methods. Following the wordline formation a thick layer of silicon dioxide 5 is deposited to a thickness approximately equal to 5000 angstroms and then planarized. The silicon dioxide 5 is masked to define future capacitor substrate contact regions with mask layer 15.

In Figure 2 the silicon dioxide 5 is anisotropically dry etched to expose the substrate 4 in the unmasked regions. Following the etch a substantially conformal first conductive layer 25, preferably a polysilicon layer having a thickness of 200-400 angstroms, is deposited to overly the exposed substrate 4 and the silicon dioxide 5. Following the formation of the conductive layer 25 upper portions of the silicon dioxide layer 5 are exposed by removing portions of the conductive layer 25 using a spacer etch or using CMP (chemical mechanical planarization) following a resist deposit. The removal of portions of the conductive layer 25 creates electrically isolated portions of the conductive layer 25. The isolated portions of conductive layer 25 are first capacitor plates of the capacitor of the invention. Conventional methods for depositing the conductive layer 25 include CVD (chemical vapor deposition), PVD (pressure vapor deposition)

and electroless deposition. In an alternate embodiment a metal layer is deposited by a conventional method and functions as the first conductive layer 25.

Following the deposition and isolation of portions of the first conductive layer 25 a conformal metal layer 30 is deposited by chemical vapor deposition to overly the first conductive layer 25 and exposed portions of silicon dioxide layer 5, see Figure 3. In a preferred embodiment the conformal metal layer 30 is titanium having a thickness of approximately 16-100 angstrom. Although in this embodiment titanium is preferred other metals may be used such as copper, gold, tungsten, and nickel. In a case where metal is used as the first conductive layer 25 it may be necessary to form diffusion barrier layer or an oxidation resistant layer or both interposed between the first conductive layer 25 and the metal layers 30. Thus, it should be noted that the first conductive layer 25 may actually be comprised of more than one material. For example in a ministack application a conductive plug and further conductive layers overlying the conductive plug may form the first conductive layer.

In Figure 4 the wafer 1 is placed in electrolytic solution 34 conducive to oxidizing the metal layer 30 when a potential is applied across the electrolytic solution 34 and the metal layer 30. The electrolytic solution 34 contacts the metal layer 30. In the preferred embodiment the electrolytic solution 34 is water, such as one part NH_4OH for 10 parts water or .1 Mole HClO_4 . However, a basic or acidic solution could also be used. A potentiostat 36 consists of a first electrode 40, known as a counter electrode, and a second electrode 45, known as a reference electrode. Both the first 40 and second 45 electrodes are emersed in the electrolytic solution 34. The potentiostat 36 also provides a third electrode 46, known as the working electrode, which is connected to the substrate 4. The substrate 4 is in electrical communication with the metal layer 30. The potentiostat 36 is a standard device, one of which is a PAR available from E.G. & G. of Princeton, New Jersey. The preferred reference electrode is an SCE (saturated calomel electrode). The potentiostat 36 monitors the current flowing between the first and third electrodes 40 and 46. The potentiostat controls the potential between the second and third electrodes 45 and 46. Preferably, the potential is in the range of -2.0 volts to 5 volts (i.e. SCE

reference electrode) for 5-120 sec depending on the desired thickness of the dielectric. The current is measured between electrodes 40 and 46 and is controlled by varying the potential between the second and third electrodes 45 and 46 to obtain the desired current. The potentiostat allows the potential to be adjusted within a range of potentials conducive to the oxidizing of titanium. The oxidation reaction simultaneously oxidizes the metal layer 30 across the entire wafer surface.

Although in the preferred embodiment a three electrode potentiostat controls the electrochemical oxidation process, a two electrode rheostat control device may also be used. However, the oxidation is less controllable using the two electrode rheostat. When using the rheostat the second electrode 45 is eliminated and the electrochemical reaction changes the counter electrode chemistry. When this happens the potential changes. Thus the oxidation of the metal layer 30 is uncontrolled. In the three electrode preferred embodiment the existence of the reference electrode provides better control of the oxidation process.

In the first embodiment substantially all of the metal layer 30 is oxidized during the electrolytic process to form a metal oxide 35, titanium dioxide in the preferred embodiment, see Figure 5. The titanium dioxide has a high dielectric constant. Preferably, the thickness of the metal oxide ranges between 10-1000 Angstroms and the dielectric constant is between 86 and 170.

Following the oxidation step the metal oxide is chemically mechanically planarized and a second conductive layer 55 is deposited to overlie the metal silicon dioxide layer 5, the silicon oxide 50 and the metal oxide 35, see Figure 6. The second conductive layer 55 is created using conventional methods such as CVD, PVD, or electroless deposition. In the preferred embodiment the conductive layer 55 is polysilicon although metal may be used instead of polysilicon, and more than one material may be used to form conductive layer 55. A mask 60 is then formed to define the future capacitor structures.

In Figure 7 the conductive layer 55 has been etched in unmasked regions to complete the capacitor structures 65. The capacitors 65 made by the method of the invention comprises a first capacitor plate which is first conductive layer 25, a second capacitor plate which is the second conductive layer 55, and a dielectric which is the metal oxide 35.

In an alternate embodiment it is only necessary to oxidize a portion of the metal layer 30 to create a metal/ metal oxide layer, or in the preferred embodiment a titanium/titanium dioxide layer. In this case the unoxidized metal layer 30 and the polysilicon layer 25 form the first capacitor plate while the thin layer of titanium oxide forms the dielectric.

In a still further alternate embodiment multiple layers of metal are deposited and at least a portion of each metal layer is electrochemically oxidized prior to the deposition of a subsequent metal layer. In this case the dielectric comprises alternate layers of oxide and metal. In this embodiment the second conductive layer 55 is deposited on the last metal oxide created.

In a second embodiment of the invention, shown in Figures 8A-12B, a first metal layer 75, such as titanium, is sputter deposited to overly the silicon dioxide layer 5 and to contact exposed portions of substrate 4 following the etch of the silicon dioxide layer 5 shown in Figure 1. The wafer 1 is then placed in an electrolytic solution of acidic water. A current flows in the electrolytic solution in response to a potential applied across the electrolytic solution. The current is controlled with a potentiostat in order to control the oxidation of the metal layer. By controlling the oxidation it is possible to oxidize only a top portion of the first metal layer 75 to form a first metal oxide 80, see Figures 9A.

Alternately the metal layer 75 is planarized to expose the silicon dioxide prior to oxidation and formation of the first metal oxide 80, see Figures 8B and 9B.

Following the first oxidation a second metal layer 85, Figure 9A, is sputter deposited to overlie the first metal oxide 80. Again the wafer 1 is placed in the electrolytic solution and an

upper portion of the second metal layer 85 is oxidized to form a second metal oxide 90, see Figures 10A and 10B.

In the alternate embodiment, shown in Figures 9B and 10B, the second metal layer 85 has been planarized to expose the silicon dioxide prior to oxidation.

Following the oxidation of the second metal layer 85 a third metal layer 95 is sputter deposited to overly the second metal oxide layer 90, and capacitors are defined by a mask 100, see Figures 11A and 11B.

Exposed first, second and third metal layers 75, 85, and 95 and exposed first and second metal oxide layers 80 and 90 are etched to form the capacitors 105 of the invention, see Figures 12A and 12B. First and third metal layers 75 and 95 form first and second capacitor plates of the capacitors 105, and the first and second metal oxide layers 80 and 90 and second metal layer 85 form the dielectric of the capacitors 105. In a preferred embodiment the first, second, and third metal layers 75, 85, and 95 are titanium. Therefore in the preferred embodiment the metal oxide layers 80 and 90 are titanium dioxide. It is also possible to use only one or to use more than the number of metal/metal oxide layers described above as the dielectric layer, or it is possible to oxidize an entire metal layer if it is not the first or last metal layer deposited.

In further conceived embodiments the metal layer 30 (in this embodiment titanium) may be alloyed with a material, such as Strontium. In this case SrTiO_3 is formed during the oxidation performed by the method of the invention. Other titanates may also be formed depending on the alloy used in combination with titanium. For Example, Ba or Pb may be combined with Ti to form BaTiO_3 and PbTiO_3 , respectively, during oxidation. The process also works for TiO_3^{-2} complexes. In a still further embodiment the metal layer 30 (in this embodiment titanium) may be oxidized in a supersaturated Sr^{+2} solution such as $\text{Sr}(\text{OH})_2$ to form SrTiO_3 , in a preferred embodiment.

The capacitors 65 and 105 shown in Figures 7 and 12(A&B) respectively are typically used in a monolithic memory device 110, such as a dynamic random access memory device, as shown in Figure 13. The monolithic memory device 110 and a processor 115 form part of a memory system 120. The processor 115 is typically used to generate external control signals which accesses the monolithic memory device 110 either directly or through a memory controller.

It will be evident to one skilled in the art that many different combinations of materials, deposits and etch steps may be used to fabricate the capacitor and dielectric of the invention without departing from the spirit and scope of the invention as claimed. The method for forming the dielectric of the invention is equally applicable to any type of capacitor structure, such as trench, container, and stacked and ministacked or variations thereof. The following patents: U.S. Patent Nos. 5,438,011 (Blalock et al.), 5,097,381 (Vo), 5,155,057 (Dennison et al.), 5,321,649 (Lee et al.), 5,196,364 (Fazan et al.), 5,381,302 (Sandhu et al.), 5,392,189 (Fazan et al.), 5,082,797 (Chan et al.), 5,134,085 (Gilgen et al.), 5,354,705 (Mathews et al.), 5,049,517 (Liu et al.), 5,053,351 (Fazan et al.), 5,061,650 (Dennison et al.), 5,168,073 (Gonzalez et al.), 5,192,703 (Lee et al), 5,262,343 (Rhodes et al.), 5,234,856 (Gonzalez), and 5,416,348 (Jeng) pertaining to the fabrication of capacitors are herein incorporated by reference. Therefore the invention is only limited by the claims.